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February 9, 2004

To: Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Req. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

| Serial No. 10/719,723 11/21/03 |

C.C. Han et al.

A METHOD TO MAKE SMALL ISOLATED FEATURES WITH PSEUDO-PLANARIZATION FOR TMR AND MRAM APPLICATIONS

## INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stole Backer 2/12/04

HT-03-007

U.S. Patent 6,493,926 to Han et al., "Bi-layer Lift-off Process for High Track Density GMR Head," discloses a method for forming a bi-layer lift-off mask for use in fabricating an abutted junction type GMR read-head sensor with a narrow trackwidth of less than 0.5 microns.

The following two U.S. Patents discuss small TMR device structures and methods for forming them:

- 1) U.S. Patent 6,562,199 to Shimazawa et al., "Manufacturing Method of Magnetoresistive Element and Film Forming Apparatus."
- 2) U.S. Patent 6,522,573 to Saito et al., "Solid-state Magnetic Memory Using Ferromagnetic Tunnel Junctions."

Sincerely,

Stephen B. Ackerman,

Req. No. 37761

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